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EXAMINER	
LANGMAN, JONATHAN C	

ART UNIT	PAPER NUMBER
1784	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/566,686	LIU ET AL.	
	Examiner	Art Unit	
	JONATHAN C. LANGMAN	1784	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,16,18-22 and 24-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,16,18-22 and 24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21, 22, 24, 25, 27, and 28 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kanel et al. ("Ballistic Electron-Emission Spectroscopy).

Regarding claims 21, 22, and 24, Kanel et al. teach a structure exhibiting diode behavior comprising a silicon substrate with a $CoSi_2$ film deposited on the entire backside of the substrate. Upon the other side of the substrate is grown a thick undoped silicon buffer layer, followed by an epitaxial deposition of Germanium dots, a thin $CoSi_2$ silicide, and then a Si cap layer, resulting in a structure comprising: backside $CoSi_2$/Si substrate/Si buffer/Germanium dots/$CoSi_2$/Si cap (pg s227, col. 2, 2nd paragraph and experimental procedure Section 1). No other layers are taught to be deposited on the backside $CoSi_2$ layer, and therefore the backside layer has a surface distal from the substrate that is exposed.

Kanel et al. is silent to the $CoSi_2$ layer inducing a tensile strain in the germanium layer, however, Kanel et al. teaches the same structure as claimed and therefore it is inherent that the $CoSi_2$ layer will increase the tensile strain of the Ge dots.

Regarding claim 25, Kanel teaches the same structure as described above, and therefore it is inherent that the structure would allow L-Band photo-detection of the Ge layer.

Regarding claims 27 and 28, Kanel et al. teach that a silicide layer is formed on a second surface of a substrate and that a Ge layer is formed over a first surface of a substrate. While there is no disclosure that the diode of Kanel et al. is a photodetector or an optical modulator, as presently claimed, applicants attention is drawn to MPEP 2111.02 which states that "if the body of a claim fully and intrinsically sets forth all the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction". Further, MPEP 2111.02 states that statements in the preamble reciting the purpose or intended use of the claimed invention must be evaluated to determine whether the purpose or intended use results in a structural difference between the claimed invention and the prior art. Only if such structural difference exists, does the recitation serve to limit the claim. If the prior art structure is capable of performing the intended use, then it meets the claim.

It is the examiner's position that the preamble does not state any distinct definition of any of the claimed invention's limitations and further that the purpose or intended use, i.e. photodetector or optical modulator, recited in the present claims does not result in a structural difference between the presently claimed invention and the prior art structure and further that the prior art structure which is a structure identical to

that set forth in the present claims is capable of performing the recited purpose or intended use.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15, 16, 18, and 19, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanel et al. (Ballistic-Electron-Emission spectroscopy") in view of Kubler et al. ("Si adatom surface migration biasing by elastic strain gradients during capping of Ge or $Si_{1-x}Ge_x$ hut islands") or Sutter et al. ("Embedding of Nanoscale 3D SiGe islands in a Si Matrix").

Regarding claims 15, 16, and 18, Kanel et al. teach a structure exhibiting diode behavior comprising a silicon substrate with a $CoSi_2$ film deposited on the entire backside of the substrate. Upon the other side of the substrate is grown a thick undoped silicon buffer layer, followed by an epitaxial deposition of Germanium dots, a thin $CoSi_2$ silicide, and then a Si cap layer, resulting in a structure comprising: backside $CoSi_2$/Si substrate/Si buffer/Germanium dots/$CoSi_2$/Si cap (pg s227, col. 2, 2nd paragraph and experimental procedure Section 1). No other layers are taught to be

deposited on the backside $CoSi_2$ layer, and therefore the backside layer has a surface distal from the substrate that is exposed.

Kanel forms a diode comprising germanium quantum dots, and then addresses the morphological changes occurring during the process of embedding Ge quantum dots in a Si matrix by using ballistic electron emission spectroscopy. Kanel teaches that dots are subjected to pronounced shape changes during Si capping and then refers to references 5 and 6 (pg s227, col. 2).

These references 5 and 6, Kubler et al. and Sutter et al., respectively, are to Germanium and SiGe quantum dots embedded in a Si matrix (see titles). It would have been obvious to one of ordinary skill in the art at the time of the present invention to substitute the germanium quantum dots of Kanel with SiGe quantum dots, in order to expand on the research started and recognized by Kanel et al., in order to address the morphological changes occurred during depositing SiGe quantum dots in a Si matrix.

Kanel et al. teaches the same structure as claimed and therefore it is inherent that the $CoSi_2$ layer will increase the tensile strain of the SiGe dots.

Regarding claim 19, Kanel teaches the same structure as described above, and therefore it is inherent that the structure would allow L-Band photo-detection of the SiGe layer.

Claims 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanel et al. ("Ballistic-Electron-Emission spectroscopy") as applied to claim 21 above, or Kanel et al. ("Ballistic-Electron-Emission spectroscopy") in view of Kubler or

Sutter, as applied to claim 15 above, and further in view of Seto et al. ("Si/SiGe resonant cavity photodiodes for optical storage applications").

Kanel teaches a diode structure however fails to teach a dielectric disposed over the germanium or silicon germanium dots.

Seto et al. teach a diode of similar structure to Kanel as seen in Figure 1. A backside contact is formed on a silicon substrate followed by a SiGe heterojunction. A dielectric stack of alternating high and low refractive index layers is disposed over heterojunction along with a top contact. Seto teaches that the dielectric stack acts as a mirror reflecting light that is not absorbed in the first pass back into the absorber layer effectively increasing the optical path length by several fold (pg 1550, and Figure 1).

It would have been obvious to one of ordinary skill in the art at the time of the present invention to dispose a dielectric stack over the SiGe or Ge layer of Kanel in order to reflect light that is not absorbed in the first pass back into the absorber in order to increase the optical path length.

Claims 15, 16, 18, 19, 21, 22, 24, 25, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selvakumar et al. (US 5,633,194) in view of Kanel et al. ("Ballistic-Electron-Emission spectroscopy"), as evidenced by Meyer et al. ("Electron and hole Focusing in CoSi2/Si(111) Observed by ballistic Electron emission Microscopy").

Regarding claims 15, 16, and 18, Selvakumar et al. teach a diode comprising a substrate 8, with a deposited layer of germanium or SiGe thereon (col. 1, lines 40-41), contacts 12 and 14 are formed on respective sides of the structure to complete the diode (see figure 5a and col. 4 lines 40-45). The aluminum layer, 14 forms an ohmic backside contact that is enhanced by phosphorous n-type doping of the substrate.

Selvakumar et al. fail to teach that the backside ohmic contact may be a silicide.

Kanel et al. teach a diode structure which includes a silicon substrate with a $CoSi_2$ film deposited on the entire backside and a $CoSi_2$/Si/Ge/Si system grown on the opposite side of the silicon substrate (s227, col. 2). Although Kanel does not refer to the backside $CoSi_2$ layer is an ohmic backside contact, further work by Kanel as well as these known structures in the art evidences that this backside layer taught by Kanel is an ohmic contact (see Meyer et al. (same inventors as Kanel), page 1520, col. 2, last five lines).

Since Kanel teaches that $CoSi_2$ is a known backside ohmic contact in the art of forming a heterojunction diode, it would have been obvious to one of ordinary skill in the art at the time of the present invention to substitute the aluminum backside ohmic contact in the diode taught by Selvakumar et al. with the $CoSi_2$ backside contact taught by Kanel as these backside contacts have been shown to be a functionally equivalent backside ohmic contact for forming heterojunction diodes.

This CoSi2 ohmic contact has a surface of the layer distal from the second surface of the substrate being exposed, as seen in Figure 5a of Selvakumar et al.

Since this structure is the same as the applicant's structure, it is inherent that the silicide layer will increase a tensile strain in the SiGe layer.

Regarding claims 19 and 25, Selvakumar as modified by Kanel teaches the same structure as described above, and therefore it is inherent that the structure would allow L-Band photo-detection of the SiGe or Ge containing layer.

Regarding claims 21, 22, and 24, as described above, Selvakumar et al. teach specific examples where SiGe is used. SiGe reads on the claimed Ge layer, as the applicant uses open ended terminology i.e. "comprising" and therefore other components may be present in the Ge layer, such as Si.

Alternatively, Selvakumar et al. teach that SiGe, Si, or Ge may be deposited on the Si substrates (col. 1, lines 40-45). It would have been obvious to one of ordinary skill in the art at the time of the present invention to substitute Ge for SiGe of the examples, as Selvakumar et al. teach that germanium is a viable alternative to SiGe.

Regarding claims 27 and 28, these claims are in product by process form, to achieve the final structure of claim 21. As described above, in the rejection of claim 21, Selvakumar et al. teach the same structure as claimed. Furthermore, the diode is formed by first forming a Ge containing film on a substrate and then forming a backside ohmic contact on the opposite surface of the substrate (see Selvakumar, col. 4, lines 36-44). These process steps are the same as claimed.

A difference between claim 21 and claims 27 and 28, is that the preamble of claims 27 and 28 sets forth that the structure is a photodetector or an optical modulator. While there is no disclosure that the diode of Selvakumar is a photodetector or an

optical modulator as presently claimed, applicants attention is drawn to MPEP 2111.02 which states that "if the body of a claim fully and intrinsically sets forth all the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction". Further, MPEP 2111.02 states that statements in the preamble reciting the purpose or intended use of the claimed invention must be evaluated to determine whether the purpose or intended use results in a structural difference between the claimed invention and the prior art. Only if such structural difference exists, does the recitation serve to limit the claim. If the prior art structure is capable of performing the intended use, then it meets the claim.

It is the examiner's position that the preamble does not state any distinct definition of any of the claimed invention's limitations and further that the purpose or intended use, i.e. photodetector or optical modulator, recited in the present claims does not result in a structural difference between the presently claimed invention and the prior art structure and further that the prior art structure which is a structure identical to that set forth in the present claims is capable of performing the recited purpose or intended use.

Claims 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selvakumar et al. (US 5,633,194) in view of Kanel et al. ("Ballistic-Electron-Emission spectroscopy"), as evidenced by Meyer et al. ("Electron and hole Focusing in

CoSi2/Si(111) Observed by ballistic Electron emission Microscopy") as applied to claims 15 and 21 above, further in view of Seto et al. ("Si/SiGe resonant cavity photodiodes for optical storage applications").

Selvakumar et al. as modified by Kanel fails to teach a diode with a dielectric layer disposed over the SiGe or Ge layer.

Seto et al. teach a diode of similar structure to Selvakumar as seen in Figure 1. A backside contact is formed on a silicon substrate followed by a SiGe heterojunction. A dielectric stack of alternating high and low refractive index layers is disposed over the SiGe layer along with a top contact. Seto teaches that the dielectric stack acts as a mirror reflecting light that is not absorbed in the first pass back into the absorber layer effectively increasing the optical path length by several fold (pg 1550, and Figure 1).

It would have been obvious to one of ordinary skill in the art at the time of the present invention to dispose a dielectric stack over the SiGe or Ge layer of Selvakumar, in order to reflect light that is not absorbed in the first pass back into the absorber in order to increase the optical path length.

Response to Arguments

Applicant's arguments with respect to claims15, 16, 18-22, and 24-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN C. LANGMAN whose telephone number is (571)272-4811. The examiner can normally be reached on Mon-Thurs 8:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on 571-272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCL

/Jennifer C McNeil/
Supervisory Patent Examiner, Art Unit 1784